Dr. Ming Liu

CAREER Summary: An entrepreneur at heart, Ming spent the past 23 years providing technical leadership in top-notch research institutes and high tech industries, and delivering innovative hardware and software solutions to customers. He is a seasoned people and project manager, an excellent team builder and a team player. He possesses strong research and problem solving skills.

SUMMARY OF QUALIFICATIONS

- Outstanding technical leader and manager in applied research with mission to commercialize scientific research.
- 20-year veteran in high tech field with proven successes in big corporations and start up environment.
- 12 years as people manager with proven track record of both people and project/program management success.
- Take initiatives to provide efficient solutions to internal and external customers.
- Risk taker with technical vision. Consistently meet project milestones.
- Work and communicate effectively with high level executives and employees.
- Build and develop team to ensure team success.
- Excellent team player with outstanding communication skills.
- Proven track record of executing complex projects that required coordination between different teams, geographical locations and companies.
- IoT system architect from device, gateway to cloud computing.
- Led hardware and software team for system and tool development.
- Familiar with FPGA and firmware development.
- Design and validate SOC chips and system boards.
- Familiar with object oriented programming methodology.
- Skilled developer in C/C++, Python, assembly, TCL, Perl, and shell script.
- Self-starter, fast learner and innovative problem solver.

TECHNICAL SKILLS

- Hardware: Electronic system design, FPGA and system design/debug, system architecture, Ethernet, Wireless, USB, SPI, I2C/SMBus/PMBus, MDIO, AXI4, ADC, data acquisition and real time processing, IoT and sensor network, embedded system design, Raspberry Pi, Arduino, MicroChip PIC microcontrollers, Software Defined Radio (SDR).
- Computer: Linux/Unix, Windows, Mac, iOS
- Software/Firmware: FPGA/CPLD firmware, embedded system programming, Python, C/C++, Visual Basic, Perl, TCL, shell scripting, assembly, OOP, MatLab, HTML/CSS, JS, SQL, MPLABX IDE, RDBMS and NOSQL Database, Numerical modeling, Hadoop/Spark and big data analytics, data visualization.
- EDA: Xilinx ISE/Vivado Design Suite, Synopsys Design Compiler / TetraMax / DFTMax / Prime Time, Mentor Graphic Tessent Product Suite, JTAG / Boundary Scan, RTL Verilog, synthesis, verification.
- Research: High performance computing, FPGA reconfigurable computing, Cyber-Physical System (CPS), IoT, Indoor localization, Sensor system integration for First Responders.

PROFESSIONAL EXPERIENCE

Applied Innovation Center, Desert Research Institute Reno, NV
Hardware, Software and Computational Technology Lead *10/15-present*

- Work with an external software vendor to design and develop web and smart phone apps for precision agriculture applications.
- Develop indoor localization solution by employing WiFi, BLE and mobile technology.
- Develop a smart water meter monitoring system by integrating Raspberry Pi, Software Defined Radio (SDR), MySQL database, Flask web applications served with uWSGI and Nginx, smart phones, cloud-based sensor fusion and data analytics.
- Lead a high caliber team of Ph.D. scientists and computer professionals to deliver WINDS^{TM} (Weather Intelligence and Numerical Decision Support) platform to private sector. Architect front end data visualization and backend big data analytics and storage.
- Pursue Federal funding opportunities (NSF, NIST, FEMA) in the area of CPS and IoT.
- Served in NSF IoT 2016 Review Panel.

ML & Associates LLC Reno, NV
Technical Consulting *10/15-present*

- Provide independent technical consulting service on hardware/software system design and development.

MoSys, Inc. Santa Clara, CA
Director of Engineering *08/09-09/15*

- Manage system bring up project for the 3rd generation of Bandwidth Engine (BE) product and work with US and Indian applications engineering team to design and implement FPGA system solutions on Xilinx Vertex7 and Ultrascale FPGA platforms as well as firmware network applications on on-chip parallel processor engines.
- Lead a hardware and software engineering team to deliver hardware/software solution for silicon debug and production ramp up.
- Design test controller on Xilinx VC707 platform employing AXI4 bus and Tri-Mode Ethernet MAC.
- Conduct project planning, resource allocation, team coordination and run weekly meeting for a cross functional team for silicon bringup.
- Architected FPGA hardware, which is capable of digital power control, supply and temperature monitoring, SD card data storage, ADC and clock source control. Device interfaces include USB, DDR, JTAG, SPI and I2C.
- Developed firmware for an embedded u-controller and PIC u-controller to perform controlling, monitoring, data communication and processing.
- Led software engineers to develop Python, TCL and C based platform to perform USB to JTAG/SPI/I2C/MDIO/GPIB interface for test control and instrument automation.
- Led the development of GUI as well as low level driver for customer demo and customer site debug.
- Architected Design for Test (DFT) for three generations of BE products and LineSpeed SERDES products.
- Hire, coach, develop and retain top notch engineering team.

Sandisk Corporation (now a brand of Western Digital) Milpitas, CA
Product Engineering Manager, 3D Memory Design *01/06-07/09*

- Managed new product development group of product and test engineers in 3D design department.
- Effectively managed project stakeholders to ensure executive project sponsorship.
- Managed test development project for 3D re-writable memory test chip. Maintain close communication with Toshiba, Japan to resolve test, characterization, and process related issues.

- Manage a team to execute a hardware/software development project on an internal tester, including hardware modification, software architecture design, and object-oriented program implementation in Visual C++.
- Managed blank media project involving a cross functional team that includes design, product/test, fab, firmware, marketing as well as offshore test house.
- Developed in-house memory programmer board using object oriented design with C++.
- Designed and developed Nintendo encryption/decryption silicon validation platform in C++.

Matrix Semiconductor, Inc. (acquired by Sandisk) Santa Clara, CA
MTS *06/02-10/05*
New Product Development Section Manager *10/05-01/06*

- Successfully validated 130nm family products on schedule.
- Developed Perl tools for Verilog - test program conversion which bridged gap between design verification and silicon validation.
- Successfully introduced 1st generation of 3D memory to production.
- Established Data Power (IBM Informix Database) infrastructure for the company. Conduct silicon data analytics for silicon yield improvement.
- Established bitmap analysis tool for wafer defect visualization.

Motorola Semiconductor Products Sector (Now Freescale) Austin, TX
Technical Staff Engineer *12/97-06/02*
Non-Volatile Memory Technology Center *11/00-06/02*

- Leading product/test engineer for TSMC embedded 0.25um split gate flash with programmable memory BIST for automotive customers.

Advanced Vehicle System Division *12/97-11/00*

- Responsible for testing and qualifying MPC555 (PowerPC core 32-bit microcontroller with embedded memory used for automotive engine control).

RSM Electron Inc. Deer Park, NY
Sr. Process Engineer *5/97-12/97*

- Conduct R&D for power semiconductor devices and packaging technology for defense industry.

Massachusetts Institute of Technology Cambridge, MA
Postdoctoral Fellow/Research Associate *9/94-5/97*

- Conduct original research on rheology and solid state reactions sponsored by NSF.
- Obtained two grants from NSF. Awarded with NSF postdoctoral fellowship.

EDUCATION

Ph.D. in Geological Sciences, 1995, Brown University, Providence, Rhode Island
M.S. in Geological Sciences, 1991, Brown University, Providence, Rhode Island
M.S. in Chemical Engineering, 1989, Chinese Academy of Sciences, Beijing, China
B.S. in Geology, 1986, Nanjing University, Nanjing, China

AFFILIATIONS

IEEE IEEE Computer Society

PUBLICATIONS

Mosenfelder, J.L., J.A.D. Connolly, D.C. Rubie, and M. Liu (2000) Strength of $(Mg,Fe)_2SiO_4$ wadsleyite determined by relaxation of transformation stress, *Physics of the Earth and Planetary Interiors*, 120(1):63-78.

Kerschhofer, L., C. Dupas, M. Liu, T.G. Sharp, W.B. Burham, D.C. Rubie, Polymorphic transformations between olivine, wadsleyite and ringwoodite: mechanisms of intracrystalline nucleation and the role of elastic strain, *Mineralogical Magazine*, vol. 62, issue 5, 617-638, 1998.

Kerschhofer, L., M. Liu, D.C. Rubie, J.D.C. McConnell, T.G. Sharp, and C. Dupas, Intracrystalline olivine-ringwoodite transformation and time-dependent growth rates, *Rev. High Pressure Sci. Technol.*, vol. 7, 28-33, 1998.

Liu, M., L. Kerschhofer, J. L. Mosenfelder, and D. C. Rubie, The effect of strain energy on growth rates during the olivine-spinel transformation and implications for olivine metastability in subducting slabs, *J. Geophys. Res.,* 103, 23897-23909, 1998.

Liu, M., J. C. Peterson, and R. A. Yund, Diffusion-controlled growth of albite and pyroxene reaction rims, *Contrib. Mineral. Petrol.,* 126, 217-223, 1997.

Liu, M., and B. Evans, Dislocation recovery kinetics in single-crystal calcite, *J. Geophy. Res.,* 102, 24802-24809, 1997.

Marone, C., and M. Liu, Transformation shear instability and the seismogenic zone for deep earthquakes, *Geophys, Res. Lett.,* 24, 1887-1890, 1997.

Liu, M., A constitutive model for olivine-spinel aggregates and its application to deep earthquake nucleation, *J. Geophy. Res.,* 102, 5295-5312, 1997.

Liu, M., and R. A. Yund, The elastic string energy associated with the olivine-spinel transformation and its implications, *Phys. Earth Planet. Int.,* 89, 177-197, 1995.

Liu, M., R. A. Yund, J. Tullis, L. Topor, and A. Navrotsky, Energy associated with dislocations: A calorimetric study using synthetic quartz, *Phys. Chem. Minerals*, 22, 67-73, 1995.

Liu, M., The elastic strain energy of coherent ellipsoidal precipitates in anisotropic crystalline solids: applications to the aragonite-calcite transformation, *MRS Proceedings*, 321, 263-270, 1993.

Liu, M., and R. A. Yund, Transformation kinetics of polycrystalline aragonite to calcite: new experimental data, modeling, and implications, *Contrib. Mineral. Petrol.,* 114, 465-478, 1993.

Liu, M., and R. A. Yund, NaSi-CaAl interdiffusion in plagioclase, *Am. Mineral.,* 77, 275-283, 1992.

CONFERENCE SPEAKER

Liu, M., *A Micromechanical Model for Transformation-induced Faulting,* Invited Speaker in Gordon Research Conference on Rock Deformation, New London, NH, Aug. 10-15, 1997.